ECR	*Exchange characters register/register*	ECR	P851M P852M P856M P857M

Syntax: [label] ⌄ ECR ⌄ r1, r2

The left and right-hand characters contained in the register specified by r2
are exchanged and then placed in the register specified by r1.
The old contents of the register specified by r2 are not changed.

Type   *Function*

T1 $(r2)_l \rightarrow r1_r$ and $(r2)_r \rightarrow r1_l$

Condition
register: Unchanged

bit	0	1			4	5			8	9	10	11			14	15
	1	1	1	0	0		r1			0	0		r2			0

Remark:
* r1 must be ≠ 0.
* Restricted to system mode if r1 = A15.

LCK		Load character with constant		LCK	P851M P852M P856M P857M

Syntax: [label] ⌴ LCK ⌴ r1, lk

The left-hand character (bits 0—7) of the constant lk is copied to bits 8—15 (right-hand character) of the register specified by r1.
Bits 0—7 of r1 remain unchanged.

Type   *Function*
T2 $lk_l \rightarrow r1_r$

Condition register: Unchanged

bit	0	1			4	5			8	9	10	11			14	15
	1	1	1	0	0		r1		0	1	0	0	0	0	0	0
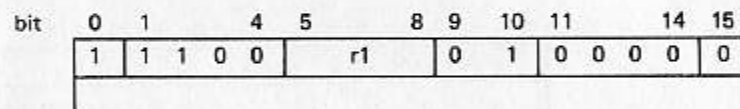
Remark:
* r1 must be ≠ 0.
* Restricted to system mode if r1 = A15.

| LCR		Load character/register		LCR	P851M P852M P856M P857M

Syntax: [label] ⌴ LCR ⌴ r1, r2

The right-hand (odd address) 8-bit contents or the left-hand (even address) 8-bit contents of the effective memory addresses, specified in r2, substitute the least significant 8 bits of the register specified by r1.
Bits 0—7 of r1 remain unchanged.

Type   *Function*
T3 $((r2))_{l/r} \rightarrow r1_r$

Condition register: Unchanged

bit	0	1			4	5			8	9	10	11			14	15
	1	1	1	0	0		r1		0	1		r2				0
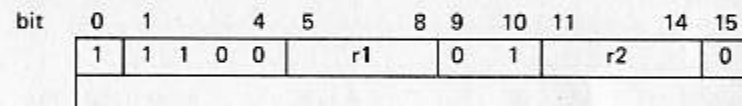
Remark:
* r1 must be ≠ 0.
* Restricted to system mode if r1 = A15.

LC — Load character

LC	*Load character*	LC

P851M
P852M
P856M
P857M

Syntax: [label] �jLC[*] � r1, m [, r2]

This instruction allows to transfer the right-hand character of the contents of the effective memory address (odd address) or the left-hand character (even address) to bits 8—15 of the register specified by r1.
Bits 0—7 of r1 remain unchanged.

Type	Function		MD	Syntax	
T4	$(m)_{l/r}$	$\to r1_r$	10	LC	r1, m
T5	$(m + (r2))_{l/r}$	$\to r1_r$	10	LC	r1, m, r2
T6	$((m))_{l/r}$	$\to r1_r$	11	LC*	r1, m
T7	$((m + (r2)))_{l/r}$	$\to r1_r$	11	LC*	r1, m, r2

Condition register: Unchanged

bit	0	1			4	5			8	9	10	11			14	15
	1	1	1	0	0		r1				MD		r2			0

Remark:
* r1 must be ≠ 0.
* Restricted to system mode if r1 = A15.

SCR — Store character/register

SCR	*Store character/register*	SCR

P851M
P852M
P856M
P857M

Syntax: [label] � SCR � r1, r2

The least significant bits of the register specified by r1 replace the right-hand (odd address) or the left-hand (even address) 8 bit contents of the effective memory address indicated by r2.

Type	Function
T3	$(r1)_r \to (r2)_{r/l}$

Condition register: Unchanged

bit	0	1			4	5			8	9	10	11			14	15
	1	1	1	0	0		r1			0	1		r2			1

Remark:
* r1 must be ≠ 0.
* Restricted to system mode if r1 = A15.

SC		*Store character*	SC	P851M
				P852M
				P856M
				P857M

Syntax: [label] ⊔ SC[*] ⊔ r1, m [, r2]

The least significant 8 bits of the register specified by r1, when address is odd, replace the right-hand 8 bits of the contents of the effective memory address or the left-hand 8 bits, when the address is even.
The unaffected half of the address remains unchanged.

Type	Function	MD	Syntax	
T4	$(r1)_r \rightarrow m, r/l$	10	SC	r1, m
T5	$(r1)_r \rightarrow m + (r2) \ l/r$	10	SC	r1, m, r2
T6	$(r1)_r \rightarrow (m) \ r/l$	11	SC*	r1, m
T7	$(r1)_r \rightarrow (m + (r2)) \ l/r$	11	SC*	r1, m, r2

Condition register: Unchanged

bit	0	1			4	5			8	9	10	11			14	15
	1	1	1	0	0		r1				MD		r2			1

Remark:
* r1 must be ≠ 0.
* Restricted to system mode if r1 = A15.

CCK		*Compare character with constant*	CCK	P851M
				P852M
				P856M
				P857M

Syntax: [label] ⊔ CCK ⊔ r1, lk

Bits 8—15 (the right-hand character) of the register specified by r1 are compared with bits 0—7 (the left-hand character) of the constant lk. The most significant bit of a character is not a sign bit. The result of the comparison is stored in the condition register.

Type	Function
T2	$(r1)_r \leftrightarrow lk_| \rightarrow CR$

Condition register:

$$CR = \begin{array}{l} 0 \ \text{if} \ (r1)_r = lk_| \\ 1 \ \text{if} \ (r1)_r > lk_| \\ 2 \ \text{if} \ (r1)_r < lk_| \end{array}$$

bit	0	1			4	5			8	9	10	11			14	15
	1	1	1	0	1		r1		0	1	0	0	0	0		1

Remark:
* r1 must be ≠ 0.
* Restricted to system mode if r1 = A15.

CCR		Compare character/register	CCR	P851M P852M P856M P857M

Syntax: [label] ⌣ CCR ⌣ r1, r2

The 8 least significant bits of the register specified by r1 are compared with the right-hand (if odd address) or left-hand (if even address) 8 bits of the contents of the effective memory address indicated in r2.
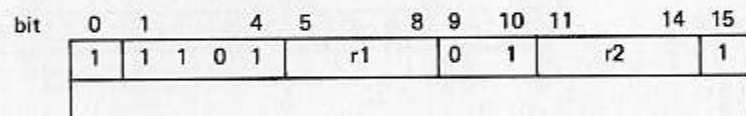The result of the comparison is stored in the condition register.
The most significant bit of a character is considered not to be a sign bit.

Type | Function
T3 | $(r1)_r \leftrightarrow \{(r2)\}_{l/r} \rightarrow CR$

Condition register:

$CR = 0$ if $(r1)_r = \{(r2)\}_{l/r}$
1 if $(r1)_r > \{(r2)\}_{l/r}$
2 if $(r1)_r < \{(r2)\}_{l/r}$

bit	0	1			4	5			8	9	10	11			14	15
	1	1	1	0	1		r1			0	1		r2			1

Remark:
* r1 must be ≠ 0.
* Restricted to system mode if r1 = A15.

CC		Compare characters	CC	P851M P852M P856M P857M

Syntax: [label] ⌣ CC [*] ⌣ r1, m[, r2]

The 8 least significant bits of the register specified by r1 are compared with the right-hand character of the contents of the effective memory address (odd address) or with the left-hand character of the contents of the effective memory address (even address).
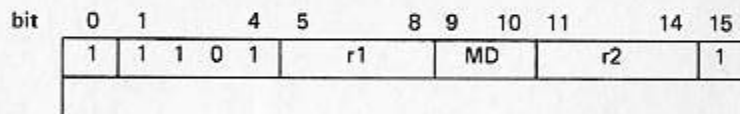The result of the operation is stored in the condition register.
The most significant bit of a character is considered not to be a sign bit.

Type	Function		MD	Syntax
T4	$(r1)_r \leftrightarrow (\ m\ )_{l/r}$	$\rightarrow CR$	10	CC r1, m
T5	$(r1)_r \leftrightarrow (\ m\ + (r2))_{l/r} \rightarrow CR$		10	CC r1, m, r2
T6	$(r1)_r \leftrightarrow ((m))_{l/r}$	$\rightarrow CR$	11	CC* r1, m
T7	$(r1)_r \leftrightarrow ((m\ + (r2)))_{l/r} \rightarrow CR$		11	CC* r1, m, r2

Condition register:

$CR = 0$ if $(r1)_r = (2nd\ operand)_{l/r}$
1 if $(r1)_r > (2nd\ operand)_{l/r}$
2 if $(r1)_r < (2nd\ operand)_{l/r}$

bit	0	1			4	5			8	9	10	11			14	15
	1	1	1	0	1		r1			MD			r2			1

Remark:
* r1 must be ≠ 0.
* Restricted to system mode if r1 = A15.