

## Preface

This volume is intended to be used together with the P800M publications concerning programming.

Part 1 describes in great detail the powerful instruction set for the P800M computers and shows the programmer the functional operation, the syntax, the setting of the condition register, the instruction time and examples.

The instructions are grouped in the following operational categories :

- Load and store instructions
- Arithmetic instructions
- Logical instructions
- Character handling instructions
- Branch instructions
- Shift instructions
- Table handling instructions
- External transfer instructions
- Control instructions
- I/O instructions
- String instructions

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**PART 1**

**INSTRUCTION SET**

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## Key to symbols used in the instruction set

Label	Identifier, or label, consisting of max. 6 characters of which the first must always be a letter. All instructions, and most of the assembler directives, may be preceded by a label.
*	Asterisk. Indicates: – indirect addressing – current value of location counter
[ ]	The syntactic item(s) between these brackets may be omitted
{ }	Choose one of the items between these brackets
r1	Register A1 . . . A15
r2	Register A1 . . . A15. Used as an index register in memory reference instructions.
r3	Register A1 . . . A7
m	Memory expression
k	Constant in bits 8–15 (short constant)
lk	Constant or address in bits 0–15 of the word following the instruction (long constant)
P	P-register. (Instruction counter)
T1	Register to register operation.
T2	Long constant instruction.
T3	Register addressing.
T3A	Register r2 is not the stackpointer A15
T3B	Register r2 is the stackpointer A15
TxS	The result must be stored in memory
T4	Direct addressing
T5	Indexed addressing
T6	Indirect addressing
T7	Indirect indexed addressing
T8	Short constant instruction
l/s	Load/store indicator. Load: bit 15 = 0 Store: bit 15 = 1
MD	Addressing mode
^	Logical AND
v	Logical OR
∨	Exclusive OR
↔	Compare
/	Divide
x	Multiply
+	Add

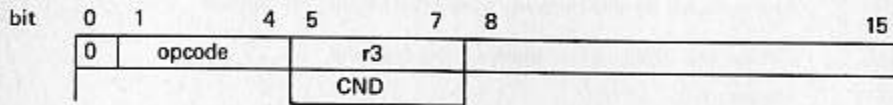
### Instruction formats

Machine instructions conform to one of the following two formats:

- format 0
- format 1.

#### Format 0 instructions

Instructions of this type consist of one word, where the 16 bits indicate the following functions :

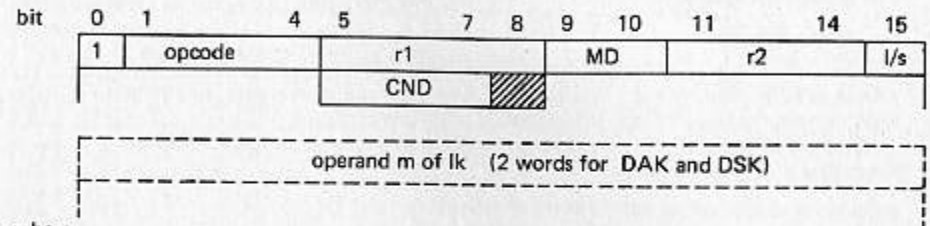


where

- bit 0 - indicates the instruction format
- bits 1-4 - operation code
- bits 5-7 - one of the registers A1-A7 or the condition value in a Branch instruction.
- bits 8-15 - the contents of this field varies according to the type of instruction and may contain one of the following values:
  - an 8-bit *positive* constant (constant instruction)
  - an even displacement value (branch instruction)
  - an indication of the shift required (shift instruction)
  - device address (I/O instruction) + function bits
  - fixed parameters (miscellaneous instruction)

#### Format 1 instructions

Format 1 instructions perform a number of operations by reference to two of the 16 registers available for user access: one of these registers may point to a data item either in a word following the instruction or elsewhere in memory as it is possible to use that register as an index register.



where:

- bit 0 - indicates the instruction format
- bits 1-4 - operation code
- bits 5-8 - one of the registers A1 . . . A15 specified as follows:
  - registers A1 . . . A7 are in group 0 and registers A8 . . . A15 are in group 1.
  - The group to which a register belongs is indicated by bit 8.
  - This may be either 0 (group 0) or 1 (group 1)
  - in branch instruction, however, bits 5 to 7 inclusive indicate a condition value and bit 8 is not used.
- bits 9-10 - addressing mode code. These bits will specify direct or indirect addressing, i.e. whether the word following the instruction, or another memory word, has to be taken into account.
- bits 11-14 - the number of one of the 16 registers, expressed in the same way as in bits 5-8.
- bit 15 - load/store indicator. Used in certain instructions to indicate that the result of the operation is to be placed either in the register shown by bits 5-8 (l/s = 0) or in a memory word (l/s = 1).

This type of instruction may be followed by a data word (16 bits) containing an address (m) or a positive or negative value. In the case of an address, bit 15 is not significant, except for character handling instructions.

The binary values of bits 5 through 8 in r1 and 11 through 14 for r2 are: 4 2 1 8, and in r3 4 2 1.

Example: A3 in r1 or r2 is written as 0110 and A12 as 1001. For r3 this is 011.  
A12 cannot be specified in the field r3.

